REMARKS

Claims remaining in the present application are 1-18. Claim 11 is amended herein. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants thank the Examiner for withdrawing the finality of the prior rejection. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

35 U.S.C. §102

Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Pole, II et al., U.S. 6,675,304 ("Pole"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-3, 5-11 and 13 are patentable over Pole.

With respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled" as recited by Claim 1.

The referenced portion of Pole alleged to teach this claimed element, column 4 lines 15-40, may describe lowering an output voltage level, but Pole fails to teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 1, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers which are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 1.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein said value of the core

voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

While Pole may teach, "chang(ing) the voltage regulator setting from a higher to a lower output level" (column 4 lines 36-38), Applicants respectfully assert that Pole fails to teach or fairly suggest that such a "lower output level" is "not sufficient to maintain processing activity in said processor" as recited by Claim 1.

In addition, the rejection's citations to Pole column 5, lines 10-16 and column 1 lines 30-34 refer to clock activity, e.g., "the external clock to the processor is disabled," but are devoid of teachings related to "core voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

For these further reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 2-3 depend from Claim 1. Applicants respectfully assert that Claims 2-3 overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to independent Claim 5, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled" as recited by Claim 5. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 5, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers which are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 5.

For this additional reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further, with respect to Claim 5, Applicants respectfully assert that Pole fails to teach or suggest the limitation:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled

as recited by Claim 5.

The underscored language refers to modes of operating a voltage regulator (power dissipation mode/power saving mode). Applicants respectfully assert that Pole fails to teach or suggest the limitations of Claim 5. Pole may discuss lowering a voltage level supplied to a processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage of a processor. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Pole is silent as to any mode of operation of a voltage regulator, aside from outputting a plurality of voltages. Consequently, Pole is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Pole fails to teach or fairly suggest the claimed transferring the operation of

a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For this further reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 6 depends from Claim 5. Applicants respectfully assert that Claim 6 overcomes the rejections of record as this claim depends from an allowable base claim, and respectfully solicit allowance of this Claim.

With respect to Claim 7, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor" as recited by Claim 7. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 7.

For this reason, Applicants respectfully assert that Claim 7 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 8-10 depend from Claim 7. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to Claim 11, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation "means for reducing the selectable voltage below a level specified by the voltage regulator" as recited by amended Claim 11.

Pole may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Pole is silent as to causing the voltage regulator to output a "voltage below a level specified by the voltage regulator," as claimed. Applicants respectfully assert that one of ordinary skill in the art would understand Pole to teach that the output voltage of the voltage regulator to be within, e.g., neither above nor below, a range specified by the voltage regulator, as Pole is silent as to causing the voltage regulator to output a voltage outside of that range.

For this reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 13, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation:

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases

as recited by Claim 13.

Applicants respectfully assert that Pole fails to teach or fairly suggest the limitations of Claim 13. The rejection asserts that Pole teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Pole does not teach or fairly suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Pole fails to teach or fairly suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

Applicants respectfully note that Pole fails to teach any coupling of the battery 60 to the voltage regulator, and thus cannot teach the claimed limitations. Further, Pole fails to teach any means for "enabling" the battery "for conserving charge stored by the voltage regulator" as recited by Claim 13.

For these many reasons, Applicants respectfully assert that Claim 13 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Pole in view of Applicants' admitted prior art ("APA") and further in view of "High-speed, Digitally adjusted step-down controllers for notebook CPUs," Maxim, July 2000, pages 1-28 ("Maxim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 4, 12 and 14-18 are patentable over Pole in view of APA and further in view of Maxim.

With respect to Claim 4, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach the limitation, "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage" as recited by Claim 4.

APA teaches, "prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a

resistor-voltage-divider network... to raise the output voltage level" (page 10 lines 6-9, emphasis added). Pole and Maxim fail to remedy this short coming.

In this manner, APA actually teaches away from embodiments in accordance with the present invention that recite using feedback to reduce an output voltage as recited by Claim 4.

For this reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 18 depends from Claim 4. Applicants respectfully assert that Claim 18 overcomes the rejections of record as this Claim depends from an allowable claim, and respectfully solicit allowance of the Claim.

With respect to Claim 12, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach or fairly suggest the limitation, "means for reducing the selectable voltage below a level provided by the voltage regulator" as recited by Claim 12.

Pole teaches throughout, "a voltage regulator 52 that regulates the supply voltage of the processor" (column 2, lines 38-40, *inter alia*). Applicants respectfully assert that a voltage supplied by a voltage regulator is inherently

supplied at, e.g., neither above or below, a level provided by the voltage regulator. Consequently, Pole teaches away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 12. Maxim and APA doe not remedy this defect.

For this reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Furthermore, Pole teaches operating a voltage regulator "within specifications" (column 4, line 8). Applicants respectfully assert that one of ordinary skill in the art would be taught away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 4 by this teaching of Pole.

For this additional reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 14, the rejection alleges that this claim contains the "same limitation as set forth in claim 12." Applicants respectfully traverse.

Applicants respectfully assert that Claims 12 and 14 set forth different embodiments in accordance with the present invention.

The rejection applies the "same rejection" to Claim 14 as was applied to Claim 12. Applicants respectfully assert that Claim 14 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 12, and respectfully solicit allowance of this Claim.

Claims 15-17 depend from Claim 14. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

CONCLUSION

Claims remaining in the present application are 1-18. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

Applicants have reviewed the following references that were cited but not relied upon and do not find these references to teach or fairly suggest the present claimed invention: US 5,5258,127, US 6,208,127, US 6,047,248, US 6,457,135, "High speed step-down controller with synchronous rectification for CPU power," Maxim, 2005, pp 1-16.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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